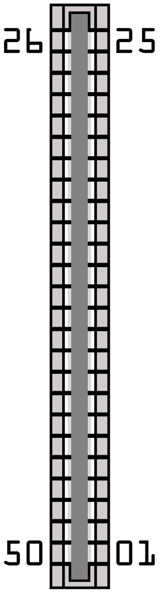
Apple II **Little Proto II**

ReactiveMicro



Congratulations on your purchase of the LittleProto II board! This high quality prototyping board will give you years of maintenance free service. We recommend using Solid 24 AWG Copper Wire, Such as “Bell Wire” that’s used to connect phones circuits.

There’s no need to worry about short circuits or excessive current situations that will hurt your Motherboard with the LittleProto II. It has four (4) built in auto-resettable fuses, one for each Power Line. They are located to the left of the Power Connectors on the upper right hand side face of the LittleProto II. Should a short circuit occur you’ll notice the Green Power LEDs will turn off. You can test these fuses by creating a short circuit, but we don’t recommend leaving the short connected for longer then 5 seconds as the fuse will start to heat up and can become quite hot. If left connected the fuse will ultimately destroy itself instead of allowing damage to occur to your system.

Note: The Apple][Bus signals have been modified over the various versions of the Apple][computer line. See notes on Pins 19, 35 and 39.
To the right is a illustration of the Apple][50 Pin Slot. It is orientated as the Top being the ‘back’ and the Bottom being the ‘front’ of your Apple][.

Pin	Name	Direction	Description (/ = Active Low Signal)	Pin	Name	Direction	Description (/ = Active Low Signal)
1	/IOSEL	OUT	I/O Select. Active when page $Cn gets accessed. N.C. on slot 0.	26	GND		System electrical ground
2	A0	IN/OUT	Buffered address bus	27	/DMAIN	OUT	Daisy-chained DMA input from higher priority devices
3	A1	IN/OUT	Buffered address bus	28	/INTIN	OUT	Daisy-chained interrupt input from higher priority devices
4	A2	IN/OUT	Buffered address bus	29	/NMI	IN	Non-Maskable Interrupt. Monitor ROM starts interrupt handling routine at location $3FB
5	A3	IN/OUT	Buffered address bus	30	/IRQ	IN	Interrupt ReQuest. Monitor starts the routine pointed to by $3FE/F
6	A4	IN/OUT	Buffered address bus	31	/RES	IN	RESet
7	A5	IN/OUT	Buffered address bus	32	/INH	IN	INHibits the on board ROMs ($D000-$FFFF)
8	A6	IN/OUT	Buffered address bus	33	-12V		-12 Volt power supply. Max 200mA for ALL peripheral boards
9	A7	IN/OUT	Buffered address bus	34	-5V		-5 Volt power supply. Max 200mA for ALL peripheral boards
10	A8	IN/OUT	Buffered address bus	35	COLORREF	OUT	Only Slot 7. 3.5 MHz Video COLOR REF. Not on Rev 0 Boards. Testpin on Slot 1 for IIe. M2B0 (IIgs)
11	A9	IN/OUT	Buffered address bus	36	7M	OUT	7Mhz clock
12	A10	IN/OUT	Buffered address bus	37	Q3	OUT	2Mhz asymmetrical clock
13	A11	IN/OUT	Buffered address bus	38	PHI1	OUT	1 MHz phase 1 clock
14	A12	IN/OUT	Buffered address bus	39	Various	OUT	USER1 on II/+: Disable address decode. 65C02 SYNC on IIe. M2SEL on IIgs.
15	A13	IN/OUT	Buffered address bus	40	PHI0	OUT	1 MHz phase 0 clock (Inverted PHI1)
16	A14	IN/OUT	Buffered address bus	41	/DEVSEL	OUT	DEVice SELect. Active when $C0nX gets accessed; n - Slot#+8
17	A15	IN/OUT	Buffered address bus	42	D0	IN/OUT	Buffered bi-directional data bus
18	R/W	IN/OUT	Buffered Read/Write signal.	43	D1	IN/OUT	Buffered bi-directional data bus
19	SYNC	OUT	Only Slot 7. SYNC from Video Generator. Not on Rev 0 Boards. Testpin on Slot 1 (IIe)	44	D2	IN/OUT	Buffered bi-directional data bus
20	/IOSTRB	OUT	I/O Strobe. Active when $C800 and $CFFF gets accessed	45	D3	IN/OUT	Buffered bi-directional data bus
21	/RDY	IN	Activation during Phi1 will halt the CPU, with the address bus holding the last address	46	D4	IN/OUT	Buffered bi-directional data bus
22	/DMA	IN	Activation disables the 6502’s address bus and halts the CPU	47	D5	IN/OUT	Buffered bi-directional data bus
23	/INTOUT	IN	Daisy-chained interrupt output to lower priority devices	48	D6	IN/OUT	Buffered bi-directional data bus
24	/DMAOUT	IN	Daisy-chained DMA output to lower priority devices	49	D7	IN/OUT	Buffered bi-directional data bus
25	+5V		+5 Volt power supply. Max 500mA for ALL peripheral boards	50	+12V		+12 Volt power supply. Max 250mA for ALL peripheral boards